WHAT IS CLAIMED IS:

1. An apparatus comprising:

a write data module to write user data, parity information, and error correction information in a memory; and

a read data module to read the user data and parity information, determine whether there is error in the user data based on the parity information, and read error correction information if there is error as determined based on the parity information.

2. The apparatus of claim 1, wherein the read data module does not read the error correction information if there is no error.

3. The apparatus of claim 1, wherein the user data and error correction information are stored in the memory such that the user data are read without reading the error correction information in the same read access to the memory.

4. The apparatus of claim 1, wherein the memory has a first set of addresses and a second set of addresses, each of the first set of addresses associated with user data, and each of the second set of addresses associated with error correction information corresponding to the user data.

5. The apparatus of claim 4, wherein each unit of user data associated with an address in the first set of addresses is shorter than 64 bits.

6. The apparatus of claim 4, wherein each address in the first set of addresses corresponds to an address in the second set of addresses, the error correction information associated with the address in the second set of addresses being used to correct one or more bits of error in the user data associated with the corresponding address in the first set of addresses if there is error in the user data.

7. The apparatus of claim 4, wherein each address in the second set of addresses is associated with more than one unit of error correction information, each unit of error correction information being used to correct one or more errors in the user data associated with an address in the first set of addresses.

8. The apparatus of claim 1, further comprising an error correction module to correct one or more errors in the user data based on the error correction information if there is error in the user data.

9. An apparatus comprising:

a write data module to write a user data unit into a first memory region of a memory, compute an error correction code unit corresponding to the user data unit, and to store the error correction code unit in a second memory region of the memory so that the user data unit can be read independently of reading the error correction code unit.

10. The apparatus of claim 9, wherein the write data module writes a plurality of user data units into a corresponding plurality of addressable locations in the first region of memory and writes a like plurality of error correction code

units into a second plurality of addressable locations in the second region of memory.

11. The apparatus of claim 10, wherein each user data unit comprises 32 bits of user data, and each error correction code unit comprises 7 bits of error correction code.

12. The apparatus of claim 9, wherein the write data module also writes a parity bit unit in the first memory region, the parity bit unit used to determine whether there is an error in the user data unit.

13. The apparatus of claim 12, further comprising a read data module to read the user data unit and the parity bit unit from the first memory region, determine whether there is an error in the user data unit based on the parity bit unit, and read the error correction code unit in the second memory region if there is an error.

14. The apparatus of claim 13, wherein the read data module does not read the error correction code unit if there is no error in the user data unit.

15. An apparatus comprising:

a memory storing a user data unit in a first memory region and an error correction code unit at a second memory region, the error correction code unit used to correct one or more bits of error in the user data unit if error occurs, the second memory region being in a different address location from the first memory region so that the user data can be read independently of reading the error correction code unit.

16. The apparatus of claim 15, wherein a plurality of user data units are stored in a corresponding plurality of addressable locations in the first region of memory, and a like plurality of error correction code units are stored in a second plurality of addressable locations in the second region of memory.

17. The apparatus of claim 15, wherein more than one error correction code unit is stored at a common address in the second memory region.

18. A network router comprising:

a network processor;

a memory; and

a memory controller in communication with the network processor having a write data module and a read data module,

the write data module to write user data, parity information, and error correction information in the memory,

the read data module to read the user data and parity information, determine whether there is error in the user data based on the parity information and read error correction information if there is error as determined based on the parity information.

19. The network router of claim 18, wherein the memory comprises static random access memory.

20. The network router of claim 18, wherein the memory controller has an error correction module to correct one or more errors in the user data based on the error correction information if there is error in the user data.

21. A method comprising:

storing user data, parity information, and error correction information in a memory;

reading the user data and parity information from the memory;

determining whether there is error in the user data based on the parity information; and

reading the error correction information if there is error as determined based on the parity information.

22. The method of claim 21, wherein the error correction information is not read if there is no error.

23. The method of claim 21, wherein storing user data, parity information, and error correction information in the memory comprises storing the user data and the error correction information in different memory regions so that the user data can be read independently of reading the error correction information.

24. A method comprising

storing user data in a first memory region; and

storing error correction information in a second memory region so that the user data can be read independently of reading the error correction information, the error correction information used to correct error in the user data.

25. The method of claim 24, further comprising writing parity information in the first memory region so that a read instruction causes the user data and corresponding parity information to be read from the memory.

26. The method of claim 25, further comprising reading the user data and the parity information, determining whether there is an error in the user data based on the parity information, and reading the error correction information if there is an error.

27. The method of claim 26, wherein the error correction information is not read if there is no error in the user data.

28. A machine-accessible medium, which when accessed results in a machine performing operations comprising:

storing user data, parity information, and error correction information in a memory;

reading the user data and parity information from the memory;

determining whether there is error in the user data based on the parity information; and

reading the error correction information if there is error as determined based on the parity information.

29. The machine-accessible medium of claim 28, which when accessed further results in the machine performing operations comprising storing the user data and the error correction information in different memory regions so that the user data can be read independently of reading the error correction information.

30. The machine-accessible medium of claim 28, which when accessed results in the machine performing operations comprising storing the user data in units less than 64 bits in the memory, and storing the error correction information in units less than 8 bits in the memory.